Zolotarev V.V., Ovechkin G.V. (Золотарев В.В., Овечкин Г.В.)

HARDWARE REPRESENTATION
of MULTITHRESHOLD DECODERS

(Moscow, Research institute of Radio, Ryazan, Ryazan state radio academy)

The development of methods of digital transmission and data processing in a large extent is determined by capabilities of systems of maintenance of high veracity of the transmitted information. The most effective means of veracity increase of the digital information is the application of noiseproof coding. The review of the most perspective coding methods by yardstick "efficiency - throughput" [1] has shown, that the greatest preference in high-velocity satellite channels the multithreshold decoders (MTD) [2]. Capabilities of these methods of error correction below are described, designed by the way of hardwares FTUE NIIR at close co-operation with other organizations and leading specialists in the field of coding systems [3,4].

CHIPset of one of designed with NIIRadio of versions of MTD implementations for convolutional code on PLIS Xilinx such as Spartan-II is rotined in a fig. 1. This MTD is development of a series of decoders of convolutional codes on the MTD basis and can be considered as the leader of their fifth decoder generation.

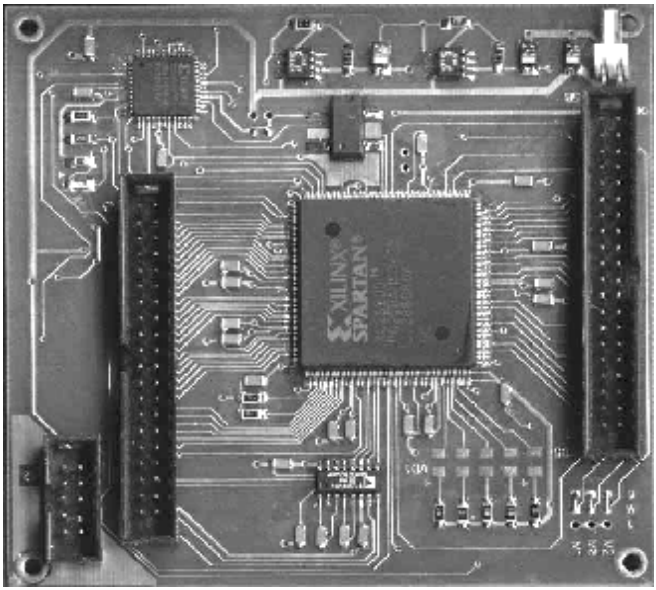

fig. 1

The characteristics PLIS of convolutional MTD at code speed R=1/2 are shown in a fig. 2 curves " МПД эксперимент (experiment) ". All capabilities of algorithms of this class on multisequencing of decoding operations at a hardware level are completely realized in it. Therefore productivity(output) of the decoder limits only by running speed of the data through its shift registers, which one fall into to the most fast members of PLIS circuitry. It also determines very much high efficiency MTD on PLIS, which one makes in the different realized versions of this decoder from 160 up to 480 Mbit/s and can be still essentially increased. Let's remark, that the data of the characteristic will well be agreed with computational results (curve "МПД модель (simulation)"), obtained by the way of statistical computer simulation.

As follows from a kind of the graphic , introduced in a fig. 2, very simple convolution МПД with response about 200 Mbit/s and with delay about 10000 bits it appears on 1,5 dB of better standard Viterbi algorithm (VA) with length of a code register K=7, the characteristics which one are submitted to a curve "АВ". Let's remind, that the improvement of a code gain (CG) even at 0,1 dB is considered as very good achievement. Therefore such large difference in CG between VA and MTD at actually unlimited decoding speed of the last one allows to approve, that the creation in NIIRadio of modern versions of MTD algorithms on the modern element base is major scientific and technological achievement in the field of noiseproof coding methods.

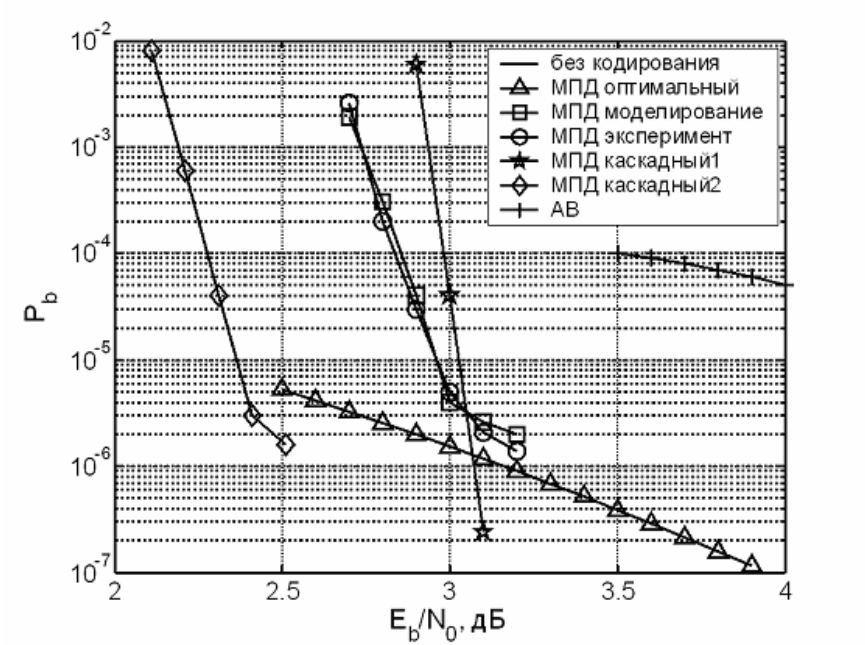

fig. 2

Well-known, that by most effective by yardstick CG are miscellaneous concatenated coding circuits. In a fig. 2 curves "МПД каскадный1" and "МПД каскадный2" show capabilities of concatenated circuits with MTD, using as an external code a code with the control on parity.

The general code rate of these concatenated circuits remains close to R~1/2, and the delay of decoding makes about 10000 bits for the first code and 40000 bits - for second. In variants of implementation of concatenated circuits throughput of the decoder exceeds 150 Mbit/s and also can be considerably increased. Let's point out, that the concatenations in MTD with a code of parity control, for what in the scheme of coding one half-adder is added only, appears many times easier, than in a concatenated circuit with VA and codes of Read - Solomon, and is effective both on CG, and on code rate.

The literature

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